VLSI/FPGA/CPLD (Transaction/Journal Papers)

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- A Discrete-Time MOS Parametric Amplifier-Based Chopped Signal Demodulator.(Trans. Nov 2020)
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- 5. A Platform of Resynthesizing a Clock Architecture into Power-and-Area Effective Clock Trees.(Trans. Oct 2020)
- 6. A Reconfigurable 64-Dimension K-Means Clustering Accelerator with Adaptive Overflow Control.(Trans. April 2020)
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- 8. An Analytical Jitter Tolerance Model for DLL-Based Clock and Data Recovery Circuits.(Trans. Nov 2020)
- 9. Gen Map: A Genetic Algorithmic Approach for Optimizing Spatial Mapping of Coarse-Grained Reconfigurable Architectures.(Trans. Nov 2020)
- 10. Low Flicker Dimmable Multichannel LED Driver With Matrix-Style DPWM and Precise Current Matching.(Trans. Nov 2020)
- 11. Low-Area and Low-Power Latch-Based Thermometer-Code Shift-Register.(Trans. Oct 2020)
- 12. Low-Cost and Power-Efficient Massive MIMO Precoding: Architecture and Algorithm Designs.(Trans. Jul 2020)
- 13. Low-Cost and Programmable CRC Implementation Based on FPGA.(Early Access July 2020)

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- Memristive Computational Memory Using Memristor Overwrite Logic (MOL) (Trans. Nov 2020)
- 15. Multi-Channel Signal Generator ASIC for Acoustic Holograms.(Trans. Jan 2020)
- 16. Performance Modeling for CNN Inference Accelerators on FPGA.(Trans. April 2020)
- 17. Phase Coherent Frequency Hopping in Direct Digital Synthesizers and Phase Locked Loops.(Trans. June 2020)
- Ultra-Low Power CMOS Image Sensor With Two-Step Logical Shift Algorithm-Based Correlated Double Sampling Scheme.(Trans. Nov 2020)
- 19. A Low-Power, High-Performance Speech Recognition Accelerator .(Trans Dec 2019)
- 20. A Low-Power Low-Cost On-Chip Digital Background Calibration for Pipelined ADCs.(Trans Nov 2019)
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